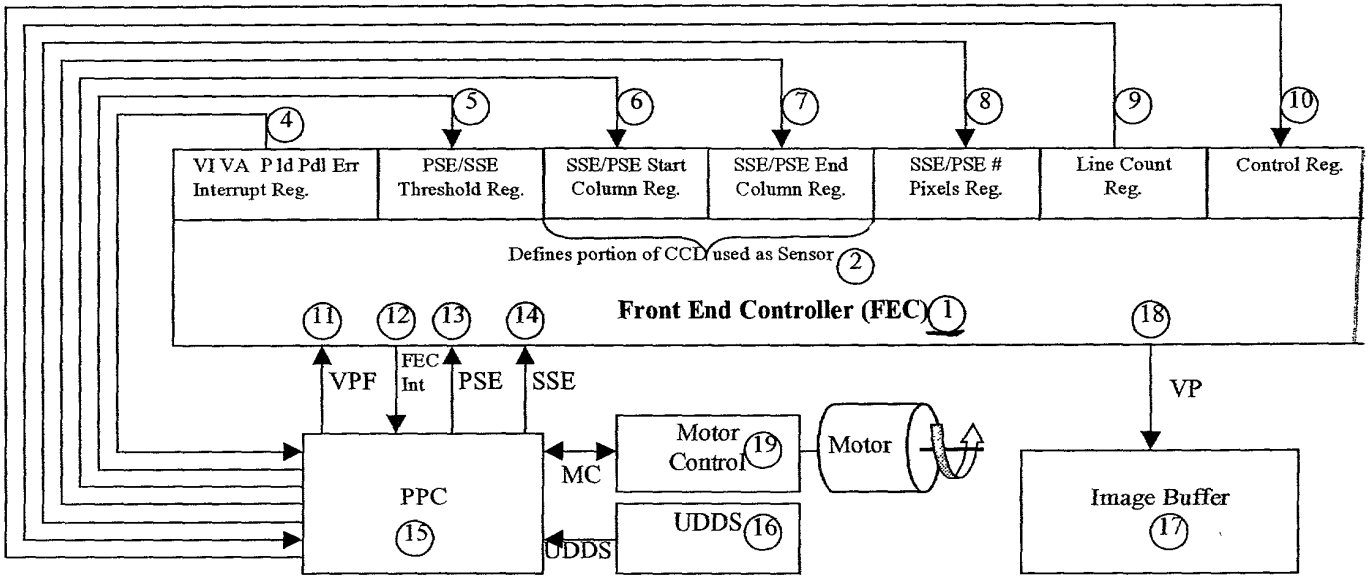
Figure 1



Key

Edge Detect: Internal FEC FPGA signal on active generates an interrupt to the Power PC & sets a bit in Int. Reg.
UDDS: Ultrasonic Document Detection Subsystem
PSE/SSE: Primary & Secondary camera Sensor Enable
PPC: Power PC CPU
VPF: Valid Page Forced
FEC Int: Front End Controller Interrupt
FEC: Front End Controller FPGA
VP: Valid Page
VA: Valid Page active
VI: Valid Page inactive
Pld: Print zone pixels detected on dark to light transition
Pdl: Print zone pixels detected on light to dark transition
Image Buffer: Image Buffer FPGA

Figure 3

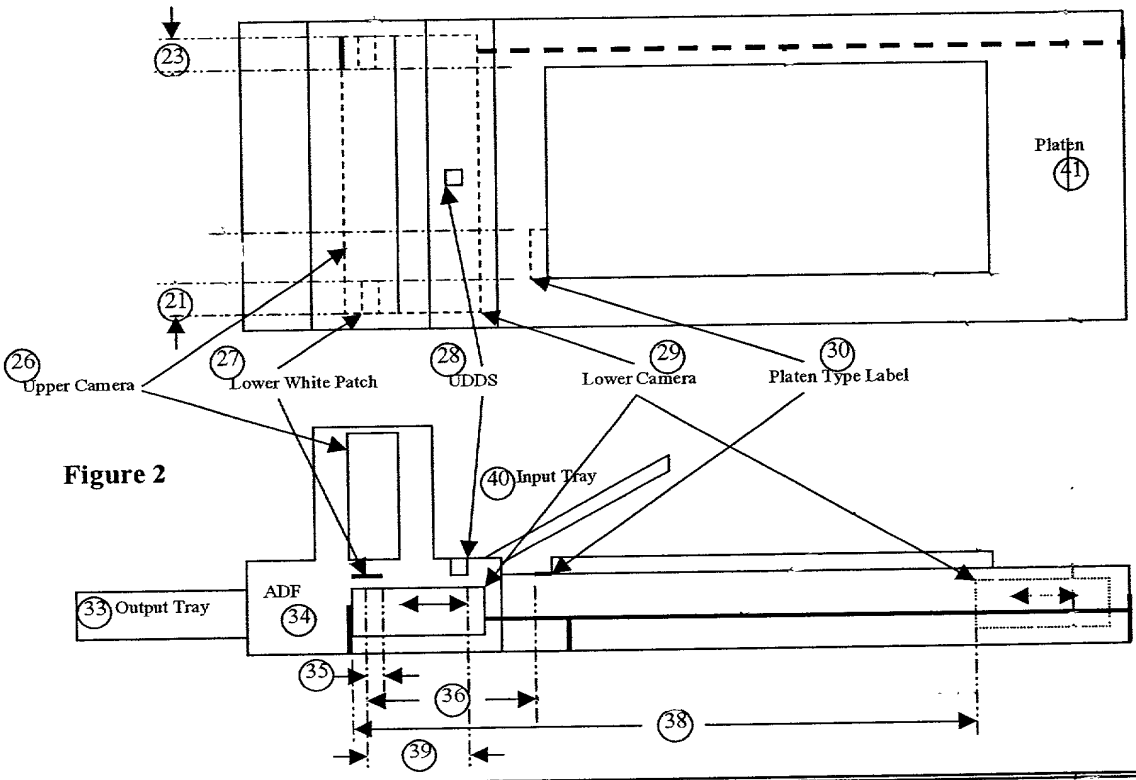


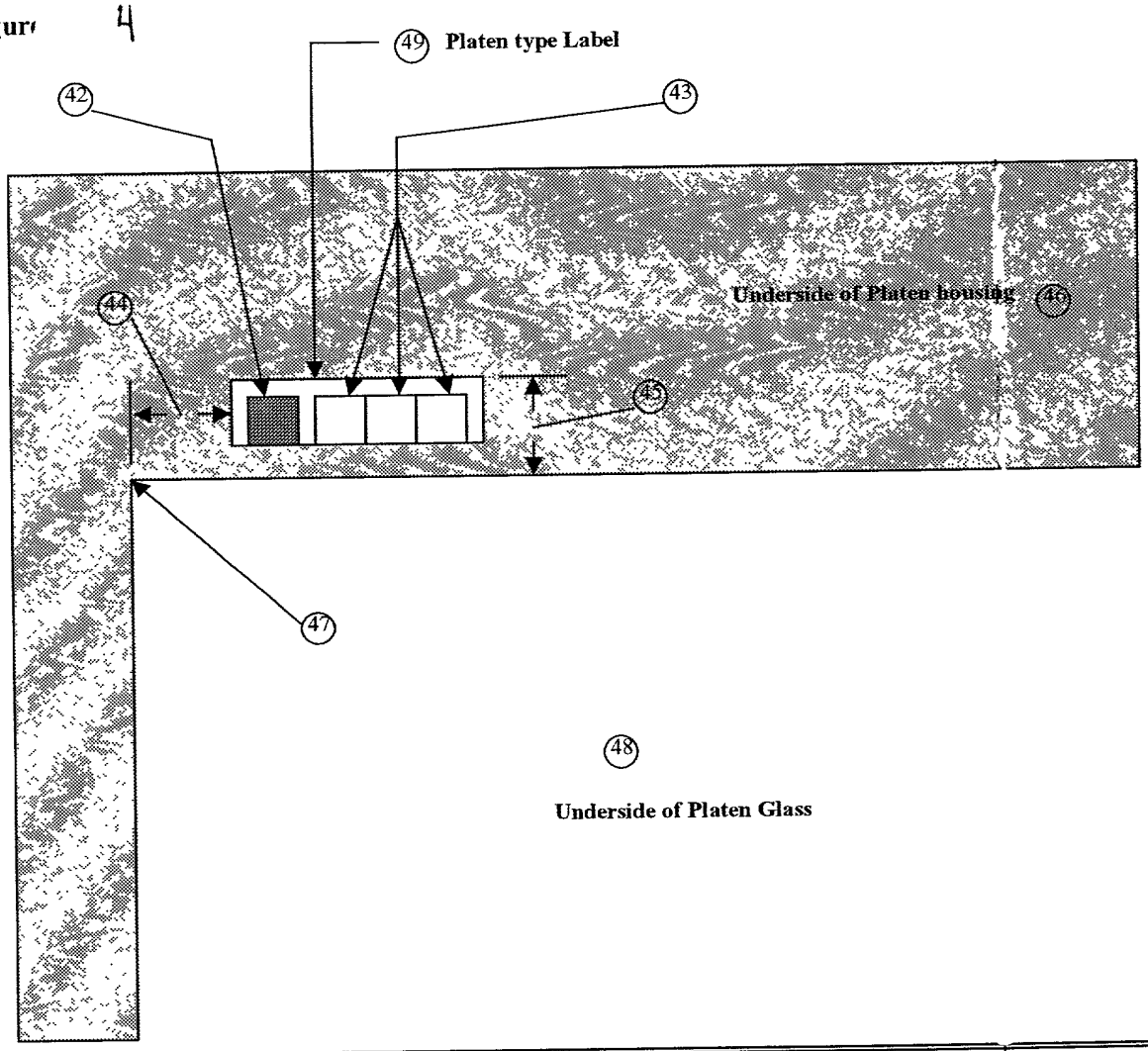
Figure 2

Key

21: Width of lower white patch
22: Width of imaging area
23: Width of upper white patch
24: Width of platen type label

35: Distance from home to edge of white patch
36: Distance from home to Platen Type Label
37: Length of scan (Depends on Platen Type)
38: Travel distance (Depends on Platen Type)
39: Distance from UDDS to CCD (Approx. 2.5")

Figur 4



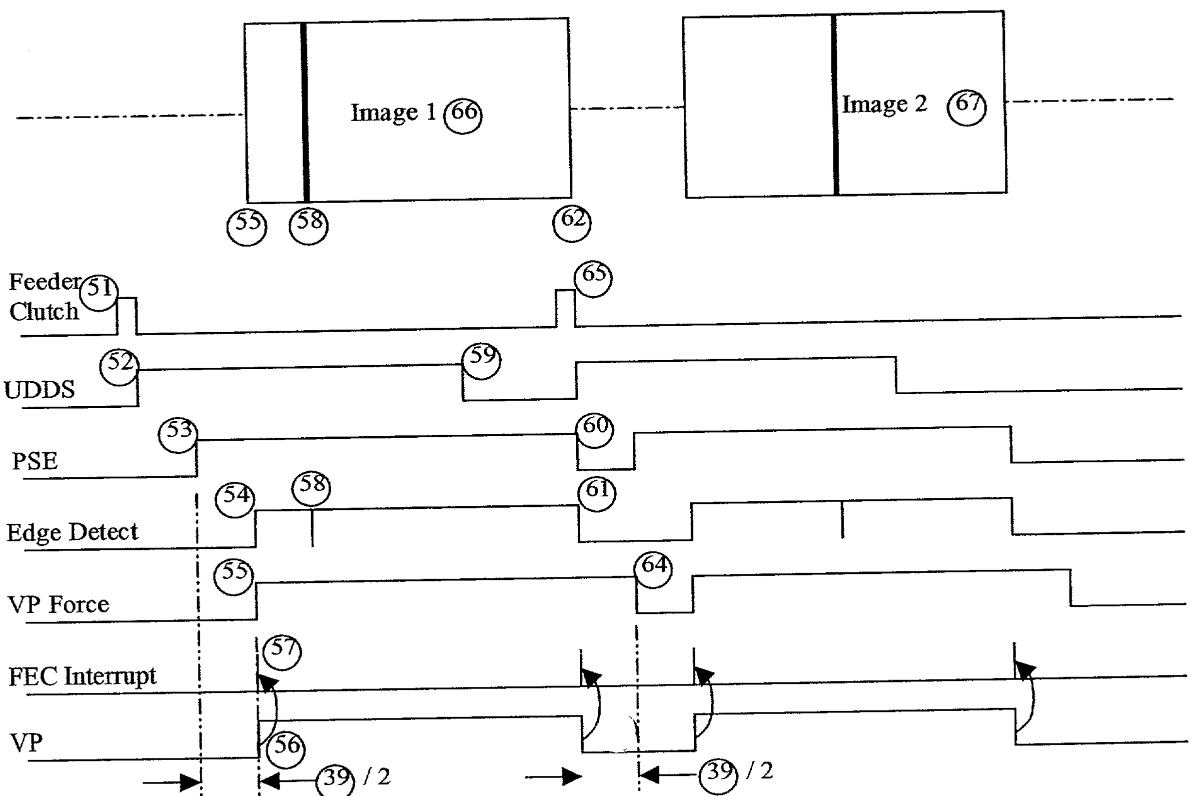
Key

49: Rectangle of light pixels of defined size and distance from item 7
42: Square area of dark pixels of defined size and location
43: Set of square areas of dark or light pixels defining Platen type
44: Distance in X direction from item 49 to item 47
45: Distance in Y direction from item 49 to item 47
46: Dark pixels defining underside of Platen
47: Document origin (upper right corner)
48: Document imaging area

Type – 0 Type – 1 Type – 2 Type – 3 Type – 4 Type – 5 Type – 6 Type – 7

Figure 5

ADF Scan of Document Fed Square



Key

Edge Detect: Internal FEC FPGA signal on active generates an interrupt to the Power PC & sets a bit in Int. Reg.

UDDS: Ultrasonic Document Detection Subsystem

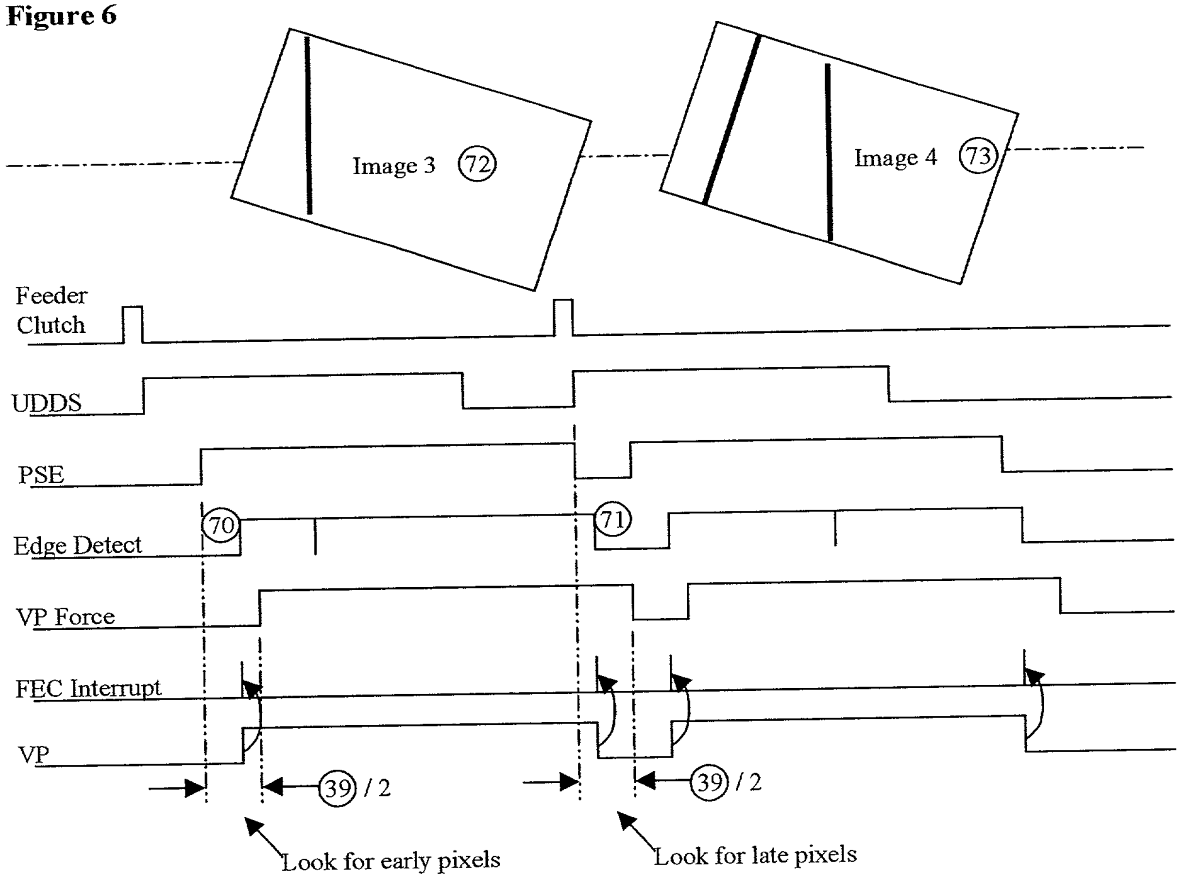
VP: Valid Page

PSE/SSE: Primary & Secondary camera Sensor Enable

VP Force: Valid Page Forced

FEC Interrupt: Front End Controller Interrupt

Figure 6



Key

Edge Detect: Internal FEC FPGA signal on active generates an interrupt to the Power PC & sets a bit in Int. Reg.
UDDS: Ultrasonic Document Detection Subsystem **VP:** Valid Page
PSE/SSE: Primary & Secondary camera Sensor Enable **VP Force:** Valid Page Forced
FEC Interrupt: Front End Controller Interrupt

Figure 7 **Platen Scan**

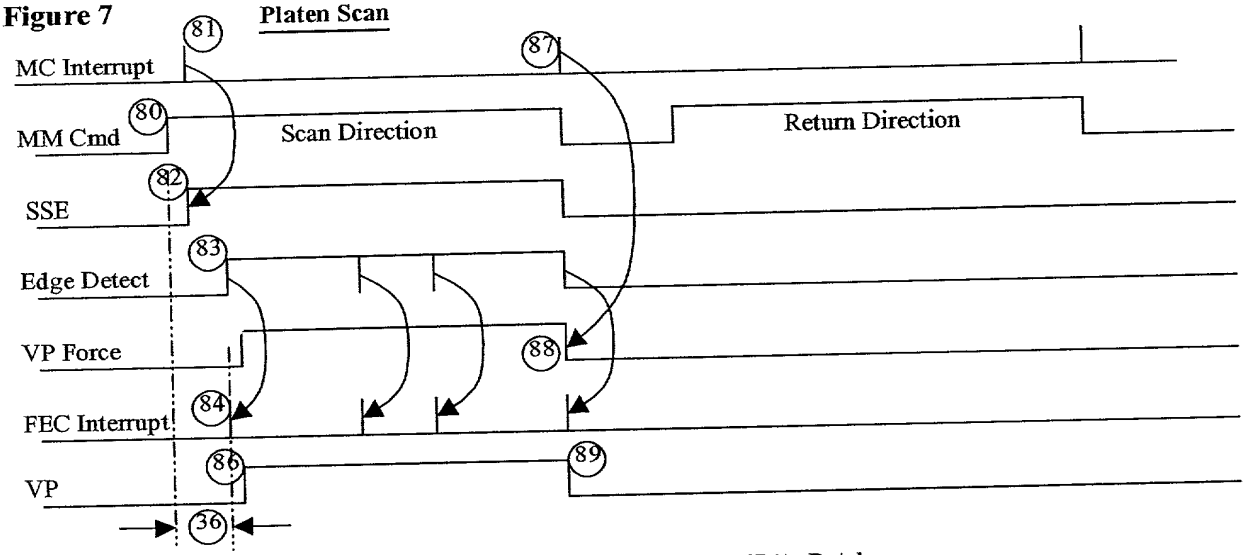
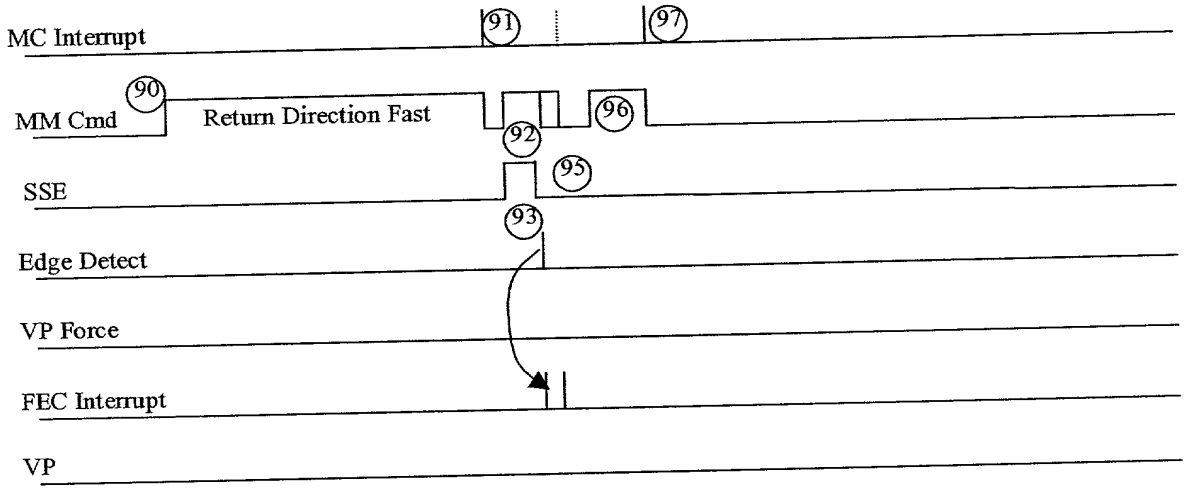


Figure 8 **Platen Home Processing Approaching White Patch**



Key

Edge Detect: Internal FEC FPGA signal on active generates an interrupt to the Power PC & sets a bit in Int. Reg.
UDDS: Ultrasonic Document Detection Subsystem **VP:** Valid Page
PSE/SSE: Primary & Secondary camera Sensor Enable **VP Force:** Valid Page Forced
FEC Interrupt: Front End Controller Interrupt **MC Interrupt:** Motor Control Interrupt
MM Cmd: Motor Move Command